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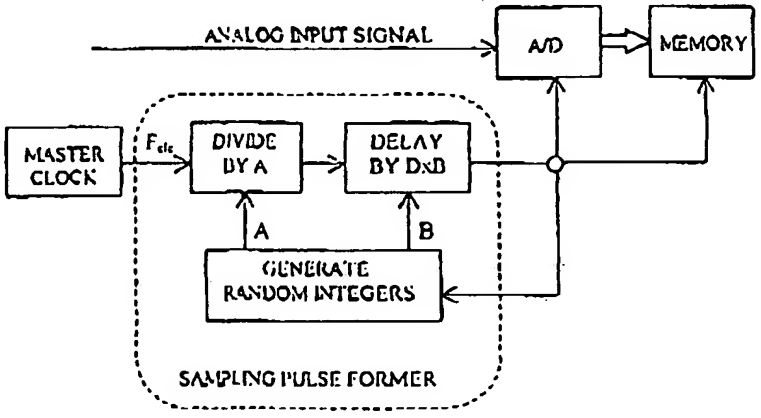
(54) Title: METHOD AND APPARATUS FOR ALIAS SUPPRESSED DIGITIZING OF HIGH FREQUENCY ANALOG SIGNALS



A schematic block diagram of the present invention

(57) Abstract: A method and apparatus for alias suppressed digitizing of high frequency analog signals, comprising sampling of the analog signals at mean frequencies considerably lower than the upper frequencies in spectra os said signals, is disclosed. A clock produces a sequence of electrical pusles at a predetermined frequency Fclk. This sequence is divided by a pseudo-random integer A to select one pulse from every series of A clock pulses. A digitally controllable delay block delays the selected pulse by a pseudo-random value DxB, where D is a constant increment of the delay and B is a pseudo-random integer. An analog-to-digital (A/D) converter samples the input signal at the time instant of the said delayed pulse. A memory receives and stores the digital sample value from the output of the A/D converter. Said integers A and B are changed after every sampling event.

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